

Appl. No. 09/976,522

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): A multi-service segmentation and reassembly (MS-SAR) integrated circuit, comprising:

- a first bus interface;
- lookup circuitry;
- segmentation circuitry;
- reassembly circuitry;
- a second bus interface; and

a data path extending from the first bus interface to the lookup circuitry, and from the lookup circuitry to the segmentation circuitry, and from the segmentation circuitry to the reassembly circuitry, and from the reassembly circuitry to the second bus interface, wherein both cell-protocol traffic and packet-protocol traffic pass over the data path from the first bus interface, through the lookup circuitry, through the segmentation circuitry, through the reassembly circuitry and out of the integrated circuit from the second bus interface, the lookup circuitry analyzing the cell-protocol traffic and outputting information that causes the cell-protocol traffic to be processed in a first way by the segmentation circuitry and the reassembly circuitry, the lookup circuitry analyzing the packet-protocol traffic and outputting information that causes the packet-protocol traffic to be processed in a second way by the segmentation circuitry and the reassembly circuitry.

Claim 2 (original): The integrated circuit of Claim 1, wherein the integrated circuit is operable in a first ingress mode such that traffic is output from the integrated circuit to a cell-based switch fabric via the second bus interface, and wherein the integrated circuit is operable in a second ingress mode such that traffic is output from the integrated circuit to a packet-based switch fabric via the second bus interface.

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Claim 3 (original): The integrated circuit of Claim 1, wherein the integrated circuit is operable in a first egress mode such that traffic is received onto the integrated circuit from a cell-based switch fabric via the first bus interface, and wherein the integrated circuit is operable in a second egress mode such that traffic is received onto the integrated circuit from a packet-based switch fabric via the first bus interface.

Claims 4 to 5 (cancelled)

Claim 6 (original): The integrated circuit of Claim 1, wherein the cell-protocol traffic is ATM traffic, and wherein the packet-protocol traffic is MPLS traffic.

Claim 7 (original): The integrated circuit of Claim 1, further comprising:
memory manager circuitry, wherein the data path extends from the segmentation circuitry to the reassembly circuitry via the memory manager circuitry.

Claim 8 (original): The integrated circuit of Claim 1, wherein the cell-protocol traffic involves an ATM cell, and wherein the packet-protocol traffic involves a packet, the ATM cell being temporarily stored in one of a plurality of buffers of a memory, all of the buffers being of equal size, the packet being segmented into a plurality of chunks, and each of the chunks being temporarily stored into a corresponding one of the buffers.

Claims 9 to 53 (cancelled)